Designing Efficient Multiplexer, Demultiplexer QCA logic circuits and Power Dissipation Analysis –A new approach

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Abstract

Quantum-dot Cellular Automata (QCA) is a creating execution innovation for the advancement of low power, low region, and very productive computerized logic circuits. QCA is an elective innovation to Complementary Metal Oxide Semiconductor (CMOS) in light of the fact that CMOS has scaling impediments which prompts high leakage power. A potential answer for the issue of rising power requests is to examine elective low power nanotechnologies for implementing logic circuits. QCA is a transistor less execution circuit. The area is the real parameter to be contrasted with different circuits amongst CMOS and QCA circuits. The proposed outline multiplexer and demultiplexers possesses $0.04 \,\mu\text{m}^2$, $0.22 \,\mu\text{m}^2$ region and 66.6% of less region contrasted with past best circuits. QCAPro software is utilized to assess energy, switching power utilization of the proposed structure.

Keywords: Binary logic circuits, Nanoscale, QCA modeling, Average Switching Energy Dissipation

1. Introduction

Over recent decades, the microelectronics business has enhanced the joining, the power utilization, and the speed of integrated circuits by methods for lessening the component size of transistors. Yet, it appears that even by reducing the CMOS transistor sizes, a few issues, for example, control utilization of power can't be controlled. It is anticipated that the scaling procedure of known-today CMOS innovation will end by the channel length of 7 nm by 2019 [1]. QCA which was first presented by Lent et al. (Loaned et al., 1993) speaks to a rising innovation at the nano innovation level.

There has been broad research as of late at nano-scale to supersede regular CMOS innovation. It is foreseen that these advances can accomplish a thickness of 1012 components/cm² and work at Tera Hertz frequencies [2] to operate the logic circuits. In request to recognize this recommendation from models of cell automata performing quantum calculations, the term has been changed to quantum-dot cellular automata (QCA). QCA is a dynamic advancement that endeavors the unavoidable nano level issues to perform computational operations. It has potential ideal conditions including fast, high device thickness, and low-power absorption [2]

Nanotechnology gives new possible results to handling in view of the fascinating properties that rise at such decrease component sizes, reduce power absorption by the devices. Quantum-speck Cellular Automata (QCA) relies upon new physical phenomena (for instance, Coulombic interaction), and innovative strategies that significantly leave from a CMOS designed electronic circuits. QCA gives an answer at nano-scale, as well as it additionally offers another strategy for calculation and data change [3-4].

2. QCA Designer Basics

A QCA cell is a nanometer size in order in which a seek permission to facilitate has four quantum dots then these quantum dots are placed four corner section of the cells. The quantum dot is a nanometer sized conductive equipment which walled in a nonconductive relevant [5], accordingly this construct may perhaps drain the electrons within threedimensional plot next stipulation an electron comes addicted to a quantum dot, exclusive of as much as necessary electrical potential required to escape electron from the quantum dot. Before injecting two further electrons addicted to a QCA unit near applying an outer potential force, these electrons possess power tunneling connecting quantum dots[6][12]. Wearing these quantum dots has a polarization furthermore these polarities symbolize the electrical incriminate of the quantum dot. Exterior inserted two electrons produce columbic interaction two different potentialities of arranged named as positive and negative polarity represents binary 1 and binary 0. QCA cell four quantum dots together utilizing burrow intersections and we can control the outer input supply of the passage intersection to lock the situation of charge or enabled signal that permits controlling the province of QCA cells to binary 0 or binary 1 position.

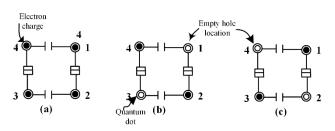
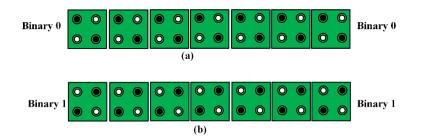


Fig. 2.1 Schematic of QCA cell (a) Electrons filled with four corners of quantum dot (b) polarization -1 level represents binary value 0 (c) polarization +1 level represents binary value 1



IJSER © 2018 http://www.ijser.org Fig. 2.2 Schematic of QCA wire (a) Binary 0 extension from beginning of wire to end point of the QCA wire (b) Binary 1 extension from beginning of wire to end point of the QCA wire

The arrangement of QCA cells next to each other appeared in figure 2.2 (a) and (b) fill in as a QCA wire. By applying binary 0 or binary 1 at one side of the wire another side of the wire same reached consequently this arrangement of QCA cells fills in as QCA wire.

QCADesigner is the most famous simulation instrument for semiconductor QCA logic circuit design[7][8]. It enables researchers to rapidly format a QCA outline and decide its usefulness in a less time period. QCADesigner assist both coplanar and multilayer intersections. In the present form, QCADesigner ver 2.0.3, there are two number of simulation engines those are bistable and coherence vector engine.

2.1 Bistable Simulation Engine

The Bistable simulation engine is executed with each cell showed as an essential two state system [9], the accompanying Hamiltonian framework can be utilized to portray the two-state framework, here kink energy between cell i and j represented by E^k , where P_j shows the polarization developed at cell j. This kink energy is related with the energy cost of two cells having inverse polarization, γ is the tunneling energy of electrons inside the cell, which is controlled by the clock frequency [10].

$$H_{i} = \begin{pmatrix} -\frac{1}{2}P_{j}E_{i,j}^{k} & -\gamma \\ -\gamma & \frac{1}{2}P_{j}E_{i,j}^{k} \end{pmatrix} \quad ----- 2.1$$

The simulation engine uses the intercellular Hartree figure (HA) to clarify a quantum mechanical structure by treating each individual cell quantum-mechanically and coupling neighboring cells in light of the Coulombic correspondence between cells. HA is a basic method to choose the consistent state of multi cell QCA systems, as it is the foundation of all QCA work that has been done in that capacity far, the stationary condition of every cell can be computed by illuminating the time-free Schrödinger condition [19].

$$H_i \Psi_i = E_i \Psi_i \quad \text{------2.2}$$

where, H_i represents Hamiltonian in above condition. Ψ_i represents state vector of the cell, and energy related with the state is E_i .

$$P_{i} = \frac{\frac{E_{i,j}^{k}}{2\gamma} \sum_{j} P_{j}}{\sqrt{1 + \left(\frac{E_{i,j}^{k}}{2\gamma} \sum_{j} P_{j}\right)}} \quad -----2.3$$

The bistable engine iteratively figures the polarization of every cell in the circuit until the point when the entire circuit merges to inside a preset capacity. By utilizing the HA strategy, the calculation just increments straightly with the quantity of QCA cells [20]. In this way, the bistable engine using HA can reproduce more QCA circuits in an amazingly capable way.

2.2 Coherence Vector Simulation Engine

In the density matrix approach, the coherence vector λ is a vector representation of the density matrix of a cell. The motion for the coherence vector including dissipative effects can be described as follows

Density matrix approach is used in coherence vector simulation and utilizes as a part of the QCA flow [21-25]. In the density matrix approach, the intelligence vector λ is a vector portrayal of the density matrix of a cell. The movement for the coherence vector including dissipative impacts can be depicted as takes after

where, $\vec{\Gamma}$ a energy vector speaking to the energy condition of the cell, is the relaxation time that is usage subordinate and $\vec{\lambda_{ss}}$ is the steady state lucidness vector.

$$\vec{\Gamma} = \frac{1}{\hbar} \left[-2\gamma, 0, \sum_{j \in s} E_{i,j}^k P_j \right] \qquad ---2.5$$

where, \hbar is the decreased Planck steady, T is the temperature in Kelvin and k_B is the Boltzmann's constant. The intelligence vector for every cell is computed by below equation utilizing an unequivocal time dependent calculation. For each time step the Γ and λ_{ss} for every cell is assessed and afterward the intelligence vector for every cell is ventured forward in time

$$\overrightarrow{\lambda_{ss}} = -\frac{\overrightarrow{\Gamma}}{\left|\overrightarrow{\Gamma}\right|} \tanh\left(\frac{\hbar\left|\overrightarrow{\Gamma}\right|}{2k_{B}T}\right) \qquad ---2.6$$



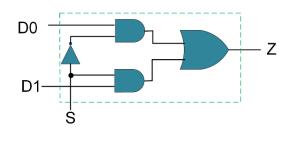
3 Simulation Parameters

In QCADesigner 2.0.3 software, the principal quantum cell was set at 18 nm by 18 nm with 5 nm distance across quantum dots. The center to focus isolate is set at 20 nm for connecting cells [26-27]. There are a few parameters that can be set by architects in the bistable engine. The aggregate reproduction is partitioned by the quantity of tests. For each example, the simulation engine takes a glance at every cell and figures its polarization in view of the polarizations of its viable neighbors that are controlled by the radius of impact.

The various parameters that are the defaults for the bistable guess are recorded as takes after[28[29] Clock low = 3.80e -23J, Convergence tolerance = 0.001, Relative permittivity = 12.90, Layer separation = 11.50 nm, Maximum iterations per sample =100, Radius of effect = 65 nm.

4. Proposed circuits implementation, simulation in QCA & Power analysis with QCAPro

In modern information acquisatation system and computerized communication application multiplexer (MUX) and demultiplexers (DEMUX) generally used to control information. To design MUX and DEMUX, qca majority gates utilized. A 2x1 (4x1) MUX have two (four) input lines and one output line, truth table represented in the table 1. The proposed 2x1 MUX configuration taken 0.04 μ m² area and requires 0.5 clock cycles with 3 majority gates, also 4x1 MUX configuration taken 0.22 μ m² area estimate and requires 1.75 clock cycles with 9 majority gates, another proposed circuit DEMUX 1x2 and 1x4 executed with qca logic gates. QCA DEMUX 1x2 involves 0.02 μ m² area and requires 0.5 clock cycles with 2 majority gates, and 1x4 DEMUX taken 0.15 μ m² area and 1.25 clock cycles delay with 8 majority gates. The composed QCA multiplexers and demultiplexer appeared in underneath figures.





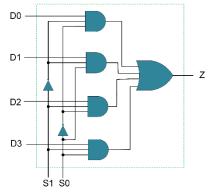


Fig. 4.2 4x1 multiplexer circuit design

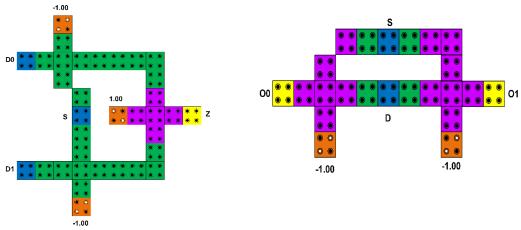
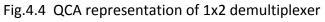


Fig. 4.3 QCA representation of 2x1 multiplexer



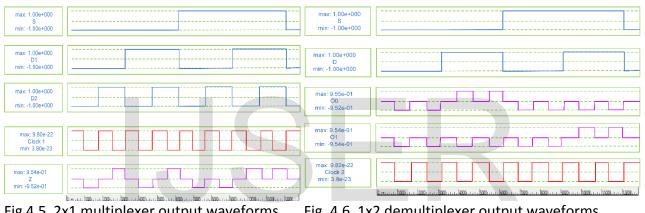


Fig 4.5 2x1 multiplexer output waveforms Fig. 4.6 1x2 demultiplexer output waveforms

Table 1: Truth table representation of 2x1 multiplexer and 1x2 demultiplexer

2X1Multiplexer					1x2 Demultiplexer					
Select line	Input Data		Output		Select line	Input	Output			
			Data			Data	Data			
S	D2 D1		Z		S	D	O1	00		
0	0	0	0		0	0	0	0		
0	0	1	1		0	1	0	1		
0	1 0		0		1	0	0	0		
0	1	1	1		1	1	1	0		
1	0	0	0							
1	0	1	0							
1	1	0	1							
1	1	1	1							

Name of the Circuit	Area (µm²)	Number of cells	Time delay in	Cross Over	
		count	terms of clock		
			cycles		
Multiplexer in [11]	0.08	46	1	coplannar	
Multiplexer in [12]	0.06	36	1	multilayer	
Multiplexer in [13]	0.07	54	1	coplannar	
Proposed Multiplexer (2x1)	0.04	29	0.5	180 ⁰ clock	
				inversion	
Multiplexer in [15]	0.25	246	1.25	coplannar	
Multiplexer in [16]	0.25	124	2	coplannar	
Multiplexer in [17]	0.15	154	1	multilayer	
Proposed Multiplexer (4x1)	0.22	193	1.75	180 ⁰ clock	
				inversion	
Proposed Demultiplexer	0.02	19	0.5	180 ⁰ clock	
(1x2)				inversion	
Proposed Demultiplexer	0.15	125	1.25	180 ⁰ clock	
(1x4)				inversion	

Table 2: Comparison table for multiplexer and demultiplexer with previous designs.

Fundamentally in the proposed circuits avoided the multi-layer crossover and whenever crossover of wires requires clock change crossover used, between clock 0 and clock 2 and clock 1 and clock 3 performed, to this sort of hybrid favorable position is area requires less, number of cells are decreases and simple to outline, primary preferred standpoint is computation of energy examination simple why in light of the fact that in multilayer frameworks control investigation can't perform.

The power dissipation by QCA circuit is figured utilizing the QCAPro programming [20][30] which one have calculation technique is upper bound dissipation model is given by

QCAPro is a displaying tool can be used to appraise the polarization error and power dissipation under sudden exchanging input levels in QCA circuits. It is realistic GUI construct tool worked in light of the Bayesian network system. The tool can assess wrong cells in substantial QCA circuit outlines by quick estimate. Keeping in mind the end goal to figure the power scattering of proposed MUX and DEMUX circuits are composed in QCADesigner 1.4.0 variant programming .qca files are inputs of QCAPro. The power dissipation is figured and seen at $0.5E_k$, $1.0E_k$, $1.5E_k$ tunnel energy level at 2⁰ k temperature and results noted in table below. Moreover with the leakage energy, average switching energy minimum and maximum energies computed.

Table 3 :	Power analysis of	multiplexer a	and	de-multiplexer	at	three	different	knick	energy
points									

		Average Leakage			Average Switching			Total Energy Dissipation		
		Energy Dissipation			Energy Dissipation			(mev)		
		(mev)			(mev)					
		0.5 E _k	1.0 E _k	1.5 E _k	0.5 E _k	1.0 E _k	1.5 E _k	0.5 E _k	1.0 E _k	1.5 E _k
MUX	2x1	0.010	0.031	0.055	0.054	0.047	0.040	0.064	0.078	0.095
	4x1	0.063	0.187	0.332	0.299	0.258	0.219	0.362	0.445	0.551
DEMUX	1x2	0.007	0.021	0.037	0.018	0.015	0.012	0.025	0.036	0.049
	1x4	0.04	0.121	0.216	0.179	0.157	0.135	0.219	0.278	0.351

Conclusion

In this paper 2x1, 4x1 MUX and 1x2, 1x4 DEMUX presented. The proposed 2x1 MUX configuration involves just 0.04 μ m² region where as the past best circuit [12] 0.06 μ m² region. Our proposed 2x1 MUX circuit requires half zone contrast with reference [11], 66.6% design area with [12] and 57.14% design area with [13]. Likewise our proposed 4x1 MUX accomplished astounding change in area however it taken more number of cells contrast with past plans. Though past best plan [16] utilizes a multilayer hybrid it isn't appropriate to discover power investigation. The proposed configuration has been examined and utilized QCAPro software. At long last the outcomes guarantee the predominance of our plan over earlier outlines as far as area, cell count, time deferral and power dissipation.

References

[1] Askari, M., M. Taghizadeh, and K. Fardad, "Design and Analysis of A Sequential Ring Counter for QCA Implementation," in *Proceedings of the International Conference on Computer and CommunicationEngineering*, 2008, pp. 933–936.

[2] Huang, J., M. Momenzadeh, and F. Lombardi, "Design of Sequential Circuits by Quantum-Dot Cellular Automata," *Microelectronics Journal*, Vol. 38, No. 4-5, 2007, pp. 525–537.

[3] Kharbash, F., and G. Chaudhry, "The Design of Quantum-Dot Cellular Automata Decimal Adder," in *Proceedings of the IEEE International Multitopic Conference*, 2008, pp. 71–75.

[4] Mardiris, V., and I. Karafyllidis, "Design and Simulation of Modular 2n to 1 QuantumDot Cellular Automata (QCA) Multiplexers," *International Journal of Circuit Theory and Applications*, Vol. 38, No. 8, 2010, pp. 771–785.

[5] Shamsabadi, A., et al., "Applying Inherent Capabilities of Quantum-Dot Cellular Automata to Design: D Flip-Flop Case Study," *Journal of Systems Architecture*, Vol. 55, No. 3, 2009, pp. 180–187.

[6] Gladshtein, M., "Quantum-Dot Cellular Automata Serial Decimal Adder," *IEEE Transactions on Nanotechnology*, Vol. 10, 2011, pp. 1377–1382.

[7] Liu, W., et al., "Cost-Efficient Decimal Adder Design in Quantum-Dot Cellular Automata," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, 2012, pp. 1347–1350.

[8] Taghizadeh, M., M. Askari, and K. Fardad, "BCD Computing Structures in QuantumDot Cellular Automata," in *Proceedings* of the IEEE International Conference on Computer and Communication Engineering, 2008, pp. 1042–1045.

[9] Yang, X., L. Cai, and X. Zhao, "Low Power Dual-Edge Triggered Flip-Flop Structure in Quantum Dot Cellular Automata," *Electronics Letters*, Vol. 46, No. 12, 2010, pp. 825–826.

[10] Vankamamidi, V., M. Ottavi, and F. Lombardi, "A Serial Memory by Quantum-Dot Cellular Automata (QCA)," *IEEE Transactions on Computers*, Vol. 57, 2008, pp. 606–618.

[11] K. Kim, K. Wu, and R. Karri, "The robust QCA adder designs using composable QCA building blocks," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 26, no.1, pp.176–183, 2007.

[12] S. Hashemi, M. R. Azghadi, and A. Zakerolhosseini, "A novel QCA multiplexer design," in Proceedings of the International Symposium on Telecommunications (IST '08), pp. 692–696, August 2008.

[13] H. Balijepalli and M. Niamat, "Design of a nanoscale quantumdot cellular automata configurable logic block for FPGAs," in Proceedings of the 2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS '12),pp.622–625, August 2012.

[14] M. Kianpour and R. Sabbaghi-Nadooshan, "A conventional design for CLB implementation of a FPGA in Quantum-dot Cellular Automata (QCA)," in Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH '12), pp. 36–42, Amsterdam, Netherlands, July 2012.

[15] V.C.Teja,S.Polisetti,andS.Kasavajjala,"QCAbasedmultiplexing of 16 arithmetic & logical subsystems-a paradigm for nano computing," in Proceedings of the 3rd IEEE International Conference on Nano/Micro Engineered and Molecular Systems (NEMS '08), pp. 758–763, Sanya, China, January 2008.

[16] M. Askari, M. Taghizadeh, and K. Fardad, "Digital design using quantum-dot cellular automata (A nanotechnology method)," in Proceedings of the International Conference on Computer and Communication Engineering (ICCCE '08), pp. 952–955, May 2008.

[17] A. M. Chabi, S. Sayedsalehi, and K. Navi, "New modules for quantum-dot cellular automata AND & OR gates," Canadian Journal on Electrical and Electronics Engineering, vol.3, no.5, pp.200–208, 2012.

[18] Dehkordi, M., et al., "Novel RAM Cell Designs Based on Inherent Capabilities of Quantum-Dot Cellular Automata," *Microelectronics Journal*, Vol. 42, 2011, pp. 701–708.

[19] A.N. Bahar, S. Waheed, M.A. Habib, A novel presentation of reversible logic gate in Quantum-dot Cellular Automata (QCA), in: 2014 International Conference on Electrical Engineering and Information Communication Technology (ICEEICT), 2014, pp. 1–6, <u>http://dx.doi.org/10.1109/ICEEICT.2014.6919121</u>.

[20] S. Srivastava, A. Asthana, S. Bhanja and S. Sarkar, "QCAPro - An error-power estimation tool for QCA circuit design," Circuits and Systems (ISCAS), 2011 IEEE International Symposium on, Rio de Janeiro, 2011, pp. 2377-2380.

[21] Ramanand Jaiswal and Trailokya Nath Sasamal , "Efficient Design of Exclusive-Or Gate using 5-Input Majority Gate in QCA" IOP Conf. Series: Materials Science and Engineering 225 (2017) 012143 doi:10.1088/1757-899X/225/1/012143

[22] Please cite this article in press as: A.N. Bahar et al., Designing efficient QCA even parity generator circuits with power dissipation analysis, Alexandria Eng. J. (2017), <u>http://dx.doi.org/10.1016/j.aej.2017.02.002</u>

[23] H. Dallaki, M. Mehran, Novel subtractor design based on quantum-dot cellular automata (QCA) nanotechnology, Int. J. Nanosci.Nanotechnology11,(2015),257–262.

[24] J.I. Reshi, M.T. Banday, Efficient design of nano scale adder and subtractor circuits using quantum dot cellular automata, in: 2016 3rd International Conference on Electrical, Electronics, Engineering Trends, Communication, Optimization and Sciences (EEECOS), 2016, pp. 89–94.

[25] K. Walus, T.J. Dysart, G.A. Jullien, R.A. Budiman, QCADesigner: a rapid design and simulation tool for quantumdot cellular automata, IEEE Trans. Nanotechnol. 3 (2004) 26.

[26] Berzon, D., and T. Fountain, "A Memory Design in QCAs Using the SQUARES Formalism," in *Proceedings of 9th Great Lakes Symposium on VLSI*, 1999, pp. 166–169.

[27] Walus, K., et al., "RAM Design Using Quantum-Dot Cellular Automata," in *Proceedings of Nanotechnology Conference*, Vol. 2, 2003, pp. 160–163.

[28] R. Jaiswal and T. N. Sasamal, "Efficient design of full adder and subtractor using 5-input majority gate in QCA," 2017 Tenth International Conference on Contemporary Computing (IC3), Noida, India, 2017, pp. 1-6. doi:10.1109/IC3.2017.8284336

[29] A.N. Bahar et al., A novel 3-input XOR function implementation in quantum dot-cellular automata with energy dissipation analysis,

Alexandria Eng. J. (2017), <u>http://dx.doi.org/10.1016/j.aej.2017.01.022</u>

[30] Taghizadeh, M., M. Askari, and K. Fardad, "BCD Computing Structures in QuantumDot Cellular Automata," in *Proceedings of the IEEE International Conference on Computer and Communication Engineering*, 2008, pp. 1042–1045.

